Favorable reconsideration of this application in light of the above amendments and the following remarks is respectfully requested. Claims 1-2 have been cancelled, claims 13-24 are pending.

A new method is provided for forming salicided surfaces to a FET device. Gate electrodes are formed including Ti/TiN salicided contact surface regions thereto. A thin layer of silicon oxide and a thick layer of photoresist are deposited. The layer of photoresist is polished, stopping on a top layer of BN of the gate electrode. The exposed layer of BN is removed. A thick layer of Ti/TiN is next deposited and annealed, forming $TiSi_x$ after which unreacted Ti/TiN is removed. A high temperature anneal is applied to reduce the sheet resistance of the layer of $TiSi_x$. As an alternate approach to the above cited sequence the layer of photoresist can be replaced with a layer of boro-phosphate-silicate-glass (BPSG), the layer of BN can be replaced with a layer of silicon nitride.

## Specification

Reconsideration of the objection to the specification under MPEP § 608.01(b) is respectfully requested based on the following.

The specification has been amended by correcting the formula for silicon nitride on page 21, line 2, of the specification in addition to other minor corrections.

In light of the foregoing response, applicant respectfully requests that the Examiner's objection to the specification under MPEP § 608.01(b) be withdrawn.

Claim Objections

Reconsideration of the claim objections is respectfully requested based on the following.

The term "creating reacted and unreacted salicide material" ahs been removed from the claims.

The term "unreacted" has been replaced in the claims with the term "un-reacted".

In light of the foregoing response, applicant respectfully requests that the Examiner's claim objections be withdrawn.

Claim rejections - 35 U.S.C. § 103(a)

1. Reconsideration of the rejection of claims 1-12 under 35 U.S.C 103(a) as being unpatentable over Pey et al. (US Patent 6,180,501) in view of Givens et al. (US Patent 5,268,330) is respectfully requested based on the following.

The rejection is considered moot because the claims have been cancelled.

In light of the foregoing response, applicant respectfully requests that the Examiner's rejection of claims 1-12 under 35 U.S.C 103(a) be withdrawn.

2. Reconsideration of the rejection of claims 1, 3, 5, 9 and 11 under 35 U.S.C 103(a) as being unpatentable over Pey et al. (US Patent 6,153,485) in view of Givens et al. (US Patent 5,268,330) is respectfully requested based on the following.

The rejection is considered moot because the claims have been cancelled.

In light of the foregoing response, applicant respectfully requests that the Examiner's rejection of claims 1, 3, 5, 9 and 11 under 35 U.S.C 103(a), be withdrawn.

3. Reconsideration of the rejection of claims 13-24 under 35 U.S.C 103(a) as being unpatentable over Pey et al. (US Patent 6,180,501 B1) in view of McAnally et al. (US Patent 6,136,700) is respectfully requested based on the following.

Pey et al. provides for the creation of a double polysilicon gate structure, the instant invention provides for a method of fabricating field effect transistors having low sheet resistance gate electrodes.

Specifically, Pey et al. provide for:

- Fig. 4, a gate electrode having a silicon nitride cap 22 and silicon nitride gate spacers 20
- Fig. 6, a layer of Ti/TiN is deposited for purposes of salicidation
- Fig. 8, after salicidation (Fig. 7) a layer 32 of TEOS is deposited and polished (Fig. 9)
- Fig. 10, and contact opening 36 is created in the layer of TEOS for access to the top of gate electrode

- Figs. 11 through 12c, a second poly gate is formed as an extension of the first poly gate 12 (40, a stud shaped additional gate in Fig. 12a; 42, a T-shaped additional gate in Fig. 12b; and 43, a relatively short stud shaped additional gate in Fig. 12c); these extended gate electrodes are show in Fig. 13a (the extended stud shape) and 13b (the T-shaped) after layer 44 of photoresist has been removed from the surface

- Fig. 13c through 15b, a thin layer 46 of Ti/Tin or Cobalt/Titanium is deposited and salicided over the extended gate structure, forming salicided layer 48, in Fig. 15a for the stud shaped extended gate structure, in Fig. 15b for the T-shaped extended gate structure and in Fig. 14c for the relatively short stud shaped extended gate structure.

The instant invention provides for, essentially following claim 13 of the instant invention:

- Figs. 8-9, providing a gate structure with salicided source/drain contact surfaces over a semiconductor substrate, a layer 17 of BN is the top layer of the gate electrode

- Fig. 9, depositing a liner layer 31 of silicon dioxide

- Fig. 9, depositing a layer 33 of dielectric over the liner layer

- Fig. 10, polishing the surface of the layer of dielectric down to the surface of the layer BN, using the layer of BN as a stop for the process of polishing
- Fig. 11, removing the layer of BN from above the one gate electrode, exposing the surface of the gate electrode
- Fig. 12, depositing a thick layer 35 of Ti/TiN as salicide material over the surface of the polished layer of dielectric including the exposed surface of the gate electrode
- Fig. 12 applying a low temperature anneal, annealing the deposited thick layer 35 of salicide material, saliciding the top surface of the gate electrode
- Fig. 13, applying a selective etch to remove un-salicided material, and
- Fig. 13, performing a high temperature anneal.

The difference between the instant invention and the invention provided by Pey et al. can best be illustrated by highlighting the steps that are provided by Pey et al. that are not part of the instant invention, as follows.

The instant invention does not provide the following steps that are provided by Pey et al.:
- providing a gate electrode having a silicon nitride cap and silicon nitride gate spacers

- depositing a layer of TEOS, the TEOS is polished
- creating a contact opening 36 through a layer of TEOS for access to the top of gate electrode
- depositing a layer of polysilicon for the formation of extended gate electrodes
- patterning and etching the deposited layer of polysilicon, forming a (extended plug shaped or T-shaped or relatively short stud shaped) second poly gate as an extension of the first poly gate
- saliciding the surface of the second poly gate.

Inversely, the instant invention provides for the following steps that are not provided by Pey et al.:

- providing the gate electrode with a top layer of BN
- depositing a layer of liner oxide over a gate electrode that has been provided with salicided source/drain surfaces
- depositing a layer of dielectric, preferably comprising photoresist, over the surface of the layer of etch stop material
- polishing the surface of the layer of dielectric down to the surface of the layer of BN, using the layer of BN as a stop for the process of polishing
- removing the layer of BN material from above the one gate electrode

- depositing a thick layer of Ti/TiN over the surface of the polished layer of dielectric including the exposed surface of the gate electrode
- performing a low temperature anneal, annealing the deposited thick layer of salicide material, saliciding the top surface of the gate electrode
- by selective etch removing un-reacted Ti/Tin, and
- performing a low temperature anneal.

Layer 110, used by McAnally as a stop layer is an etch stop layer, which is not related to a polish stop layer as provided by the instant invention. The key aspects of the instant invention are the use of the layer 17, Fig. 9, of BN as a cap layer for the polysilicon gate in addition to the application of a layer 31 of silicon oxide and the dielectric 33, Fig. 9, preferably comprising photoresist.

The advantages that are provided by these key aspects of the instant invention are that, since the polishing selectivity for photoresist and silicon oxide ($PR/SiO_2$) is larger than about 30 and the polishing selectivity for photoresist/BN (PR/BN) is larger than about 200, the polishing process can safely stop on the layer 17 of BN, in this manner preventing the typical corrosion of a conventional process.

In light of the foregoing response, applicant respectfully requests that the Examiner's rejection of claims 13-24 under 35 U.S.C 103(a) as being unpatentable over Pey et al. (US Patent 6,180,501) in view of McAnally et al. (US Patent 6,136,700), be withdrawn.

The prior art made of record and not relied upon that is considered pertinent to Applicant's disclosure, that is Poon et al. (US Patent 5,064,683), Stanley Wolf's "Silicon Processing for the VLSI Era", Buynoski (US Patent 6,187,675) and Huster et al. (US Patent 6,391,767) have been examined and have been found to be of general interest to the invention. These prior art records however do not teach the extent and the detail combined with the flexibility of the present patent application.

## Other Considerations

No new independent or dependent claims have been written as a result of this office action, no new charges are therefore incurred due to this office action.

## SUMMARY

A new method is provided for forming salicided surfaces to a FET device. Gate electrodes are formed including Ti/TiN

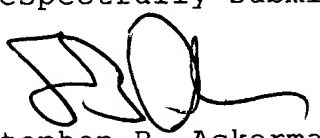
salicided contact surface regions thereto. A thin layer of silicon oxide and a thick layer of photoresist are deposited. The layer of photoresist is polished, stopping on a top layer of BN of the gate electrode. The exposed layer of BN is removed. A thick layer of Ti/TiN is next deposited and annealed, forming $TiSi_x$ after which unreacted Ti/TiN is removed. A high temperature anneal is applied to reduce the sheet resistance of the layer of $TiSi_x$. As an alternate approach to the above cited sequence the layer of photoresist can be replaced with a layer of boro-phosphate-silicate-glass (BPSG), the layer of BN can be replaced with a layer of silicon nitride.

It is requested that should Examiner not find the claims to be allowable that he call the undersigned Attorney at his convenience at 845-452-5863 to overcome any problems preventing allowance.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned:

**"Version with markings to show changes made."**

Respectfully submitted,



Stephen B. Ackerman (Reg. No 37,761)

**Version with markings to show changes made**

IN THE SPECIFICATION

1) page 3, last paragraph, please replace this paragraph with the following:

For advanced FET devices, which have a channel length of 0.25 μm or less, it is difficult for the conventional process of salicidation [the] to simultaneously meet the requirements of ultra shallow junction depth and of low sheet resistivity of the surface of the contact regions. Junction leakage can be reduced by reducing the thickness of the layer of silicide, this however increases the sheet resistivity. The invention provides a method that addresses these concerns.

2) page 4, third paragraph, please replace this paragraph with the following:

A principle objective of the invention is to provide a [methods] method of salicidation whereby uniform polishing of the salicided surfaces is maintained.

3) page 4, last paragraph, please replace this paragraph with the following:

Yet another objective of the invention is to provide a [methods] method of salicidation whereby polishing of the salicided surface can be performed using relatively relaxed parameters of polishing time, that is providing a relatively wide "processing window" for the polishing operation.

4) page 15, second paragraph, please replace this paragraph with the following:

The metal contacts with the source/drain regions and the gate electrode are formed as a final step. A dielectric 30' such as silicon oxide is blanket deposited over the surface of the created structure, patterned and etched to create contact openings 36'/37' over the source/drain regions and opening 38' over the top surface of the gate electrode. The [metalization] metallization layer selectively deposited over the patterned dielectric establishes the electrical contacts 40'/42' with the source/drain regions and 44' with the top surface of the gate electrode.

5) page 18, third paragraph, please replace this paragraph with the following:

After the gate structure 14/16 has been formed[.] LDD implants 18 are performed in order to reduce or eliminate the occurrence of leakage current between the gate electrode and the underlying silicon substrate. As typical LDD implant conditions can be cited an LDD implant for a NMOS device using arsenic with an energy within the range of between 1 to 10 keV and a dose within the range of between 1e14 to 1e16 atoms/$cm^2$. Also, an LDD implant for a PMOS implant using $BF_2$ with an energy within the range of between 1 to 10 keV and a dose within the range of between 1e14 to 5e15 atoms/$cm^2$.

6) page 21, third paragraph, please replace this paragraph with the following:

Next, Fig. 3, a silicon nitride liner 30 is deposited. The layer 30 of silicon nitride [($Si_3Ni_4$)] <u>($Si_3N_4$)</u> can be deposited using LPCVD or PECVD procedures at a pressure between about 200 mTorr and 400 mTorr, at a temperature between about 600 and 800 degrees C., to a thickness of about 1500 to 3000 Angstrom using $NH_3$ and $SiH_4$ or $SiCl_2H_2$. The silicon nitride layer 30 can also be deposited using LPCVD or PECVD procedures using a reactant gas

mixture such as dichlorosilane ($SiCl_2H_2$) as a silicon source material and ammonia ($NH_3$) as a nitrogen source, at a temperature between about 600 and 800 degrees C., at a pressure between about 300 mTorr and 400 mTorr, to a thickness between about 200 and 300 Angstrom.

7) page 22, third paragraph, please replace this paragraph with the following:

The surface of layer 32 of BPSG is then polished using methods of CMP, down to the surface of layer 30 of silicon nitride, using the surface of layer 30 [of] as the stop layer for the CMP process. This results in the cross section that is shown in Fig. 4.

8) page 22, last paragraph, page 23, first paragraph, please replace this paragraph with the following:

In the cross section that is shown in Fig. 4, it is clear that the surface of the layer 30 of silicon nitride is exposed where this layer overlays the gate electrode structure 14/16. This makes it possible to etch the layer 30 of silicon nitride over this exposed surface region and [removing] to remove the

silicon nitride of layer 30 from above the gate electrode structure 14/16.

9) page 48, please replace ABSTRACT

[A new method is provided for forming salicided surfaces to a FET device. Gate electrodes are formed, consisting, for the first embodiment of the invention, of stacked layers of silicon oxide (pad oxide), polysilicon and boronitride (BN). A thin layer of Ti/TiN is deposited, a low temperature anneal is performed. A selective wet etch removes unreacted Ti/TiN, a thin layer of silicon oxide is deposited. A thick layer of photoresist is deposited. The layer of photoresist is polished, stopping on the layer of BN. The surface of the layer of BN is now exposed, the layer of BN is removed. A thick layer of Ti/TiN is next deposited, filling the opening from where the layer of BN has been removed. A low temperature anneal anneals the layer of Ti/TiN, forming $TiSi_x$. The unreacted Ti/TiN is removed with a selective wet etch, leaving the layer of thick $TiSi_x$ in place overlying the gate electrode. A high temperature anneal is applied to reduce the sheet resistance of the layer of $TiSi_x$. As an alternate approach to the above cited sequence, forming the second embodiment of the invention, the function of the layer of photoresist can be replaced with a layer of boro-phosphate-

silicate-glass (BPSG), the function of the top layer of BN can be replaced with a layer of silicon nitride.]

with the following new ABSTRACT:

A new method is provided for forming salicided surfaces to a FET device. Gate electrodes are formed including Ti/TiN salicided contact surface regions thereto. A thin layer of silicon oxide and a thick layer of photoresist are deposited. The layer of photoresist is polished, stopping on a top layer of BN of the gate electrode. The exposed layer of BN is removed. A thick layer of Ti/TiN is next deposited and annealed, forming $TiSi_x$ after which unreacted Ti/TiN is removed. A high temperature anneal is applied to reduce the sheet resistance of the layer of $TiSi_x$. As an alternate approach to the above cited sequence the layer of photoresist can be replaced with a layer of boro-phosphate-silicate-glass (BPSG), the layer of BN can be replaced with a layer of silicon nitride.

IN THE CLAIMS

Claims 1-12: Please cancel claims 1-12.

13. (Amended) A method of fabricating field effect transistors having low sheet resistance gate electrodes, comprising the steps of:

providing a semiconductor substrate, said substrate having been provided with at least one gate electrode created over an active surface region as said substrate as defined by regions of Shallow Trench Isolation provided in the surface of the said substrate, said at least one gate electrode having been provided with gate spacers, impurity implants of source and drain regions in addition to Lightly Doper Diffusion regions having been provided in the surface of said substrate self-aligned with said at least one gate electrode, said at least one gate electrode comprising a stack of layers of pad oxide created over the surface of said substrate, a layer of polysilicon patterned over the layer of pad oxide and a layer of boronitride patterned over the layer of polysilicon;

depositing a thin layer of salicide material over the surface of said substrate, including the surface of said gate spacers and said layer of polysilicon provided for said at least one gate electrode;

performing a first anneal[, creating reacted and unreacted salicide material], forming salicided layers comprising [said] reacted salicide material over the surface of said source and drain implants;

first removing [said unreacted] un-reacted salicide material from the surface of said substrate;

depositing an isolation film over the surface of said substrate, including the surface of said gate spacers and said layer of boronitride provided for said at least one gate electrode;

depositing a layer of filler material over the surface of said isolation film to [an adequate] a thickness such that the surface of said layer of filler material extends above the surface of said isolation film even where said isolation film overlays the surface of said at least one gate electrode;

polishing the surface of said layer of filler material and said layer of isolation film down to the surface of said layer of boronitride of said at least one gate electrode, using said layer of boronitride as a stop for said process of polishing;

removing said layer of boronitride from said at least one gate electrode, exposing the surface of said layer of polysilicon forming part of said at least one gate electrode;

depositing a thick layer of salicide material over the surface of said polished layer of filler material, including the exposed surface of said layer of polysilicon;

performing a second anneal of said deposited thick layer of salicide material[, creating reacted and unreacted salicide

material], a layer of reacted salicide material overlying said layer of polysilicon of said at least one gate electrode;

second removing [unreacted] un-reacted salicide material from the surface of said layer of dielectric;

performing a third anneal, reducing the sheet resistance of said reacted salicide material overlying said layer of polysilicon of said at least one gate electrode.

16. (Amended) The method of claim 13 wherein said first removing said [unreacted] un-reacted salicide material from the surface of said substrate comprises performing a selective wet etch.

22. (Amended) The method of claim 13 wherein said second removing [unreacted] un-reacted salicide material from the surface of said layer of filler material comprises performing a selective wet etch.

24. (Amended) A method of fabricating field effect transistors having low sheet resistance gate electrodes, comprising the steps of:

providing a semiconductor substrate, said substrate having been provided with at least one gate electrode created over an active surface region as said substrate as defined by regions of Shallow Trench Isolation provided in the surface of the said

substrate, said at least one gate electrode having been provided with gate spacers, impurity implants of source and drain regions in addition to Lightly Doper Diffusion regions having been provided in the surface of said substrate self-aligned with said at least one gate electrode, said at least one gate electrode comprising a stack of layers of pad oxide created over the surface of said substrate, a layer of polysilicon patterned over the layer of pad oxide and a layer of boronitride patterned over the layer of polysilicon;

depositing a thin layer of Ti/TiN over the surface of said substrate, including the surface of said gate spacers and said layer of polysilicon provided for said at least one gate electrode, deposited to a thickness between about 100 and 500 Angstrom and more preferably to a thickness of about 300 Angstrom;

performing a low temperature anneal of said deposited thin layer of Ti/TiN in a temperature range of between about 600 and 850 degrees C. for a time between about 20 and 60 seconds, creating a layer of $TiSi_x$ over the surface of said source and drain implants, leaving uncreated Ti/TiN in place over the surface of said Shallow Trench Isolation regions;

removing said uncreated Ti/TiN from the surface of said substrate by performing a selective wet etch;

depositing a layer of silicon oxide over the surface of said substrate, including the surface of said gate spacers and said layer of boronitride provided for said at least one gate electrode;

depositing a layer of photoresist over the surface of said layer of silicon oxide to [an adequate] a thickness such that the surface of said layer of photoresist extends above the surface of said layer of silicon oxide even where said silicon oxide overlays the surface of said at least one gate electrode;

polishing the surface of said layer photoresist and said layer of silicon oxide down to the surface of said layer of boronitride being part of at least one gate electrode, using said layer of boronitride as a stop for said process of polishing;

removing said layer of boronitride from said at least one gate electrode by applying an Reactive Ion Etch, exposing the surface of said layer of polysilicon forming part of said at least one gate electrode;

depositing a thick layer of Ti/TiN over the surface of said polished layer of photoresist, including the exposed surface of said layer of polysilicon, deposited to a thickness between about 2,000 to 5,000 Angstrom ;

performing an anneal of said deposited thick layer of Ti/TiN by rapid thermal annealing in a temperature range of

between about 600 and 850 degrees C. for a time between about 20 and 60 seconds, creating a layer of $TiSi_x$ overlying said layer of polysilicon of said at least one gate electrode;

removing [unreacted] un-reacted Ti/TiN from the surface of said layer of photoresist by performing a selective wet etch;

performing an anneal of said layer of $TiSi_x$ overlying said layer of polysilicon of said at least one gate electrode, comprising a rapid thermal annealing in a temperature range of between about 850 and 1000 degrees C. for a time between about 20 and 60 seconds, reducing the sheet resistance of said reacted salicide material overlying said layer of polysilicon of said at least one gate electrode.